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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,775	02/02/2004	Srinivasa Chakravarthy	TI-29660.1	5166

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EXAMINER	
CHASE, SHELLY A	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,775	CHAKRAVARTHY ET AL.	
	Examiner	Art Unit	
	Shelly A. Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-14* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 14 are presented for examination. Receipt is acknowledge of preliminary amendment filed 2-2-2004.

Priority

2. This application appears to be a division of Application No. 09/681598, filed may 04, 2001. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because of the identification of elements by numbers in parenthesis, please remove.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 to 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over De et al. (USP 5903578) in view of Whetsel (USP 6223315 B1).

Claims **1** and **5**:

De substantially teaches a method for testing an ASIC embedded core that includes proprietary and nonproprietary circuit as well as customer supplied circuitry wherein a software program generates patterns to test the core (see col. 1 line 12 et seq.); the method comprising the steps of: using a partial netlist created by removing gates during a structural analysis (see col. 5, lines 36 to 45), an automatic test pattern generator generates test patterns to test part of the core as well as other parts of the ASIC while protecting the intellectual property data of the core (see col. 4, lines 54 et

seq.). De also teaches that scan flip-flops acts as pseudo inputs and pseudo outputs (see col. 5, lines 55 to 60).

De further teaches that the test shells use a single test port that includes an input line, output line and a control line (see col. 5, lines 10 to 15) and a serial scan port for testing the core (see col. 6, lines 54 to 60). De teaches that the ASIC vendor generates test vectors to be applied to the core via the test port (see col. 6, lines 52 to 62). De teaches that the core can be tested using scan test and vectors generated by the ASIC vendor (see col. 6, lines 63 et al.)

De also teaches testing the ASIC embedded core using a combination of the customer supplied test vectors and the partial netlist through a scan test process and a generation software tool (see col. 8, lines 33 et seq.). De does not clearly that an output node connected to an input node of a netlist represents said customer supplied circuitry; however, Whetsel in an analogous art teaches testing an integrated circuit with an IP core using a TAP interface (39) for accessing a user-added scan register (25) wherein all instructions are included in the TAP (see fig. 4 and col. 3, lines 20 et seq.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ASIC of De to include a user-added scan register as taught by Whetsel since, Whetsel teaches testing an IC with an embedded core and a user-added scan register provides greater flexibility in testing embedded cores. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have been motivated to employ a method wherein a customer has greater flexibility of testing an embedded core.

As per claims **2** and **6**, De teaches that a scan chain used to test the integrated circuit provides pseudo input (see col. 5, lines 55 to 64).

As per claims **3** and **7**, De teaches an automatic test-generating program generating test vectors to test the integrated circuit using the netlist (see col. 5, lines 20 to 35).

As per claims **4** and **8**, De teaches an integrated circuit with an embedded core including proprietary circuitry; however, De fails to clearly tech that the embedded core includes a JTAG interface. Whetsel teaches an embedded core including a test access port (TAP) (see fig. 4 and col. 3, lines 33 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ASIC of De to include a test access port interface as taught by Whetsel since, Whetsel teaches that testing an IC including an embedded core with a test access port is a known standard in the art and permits reuse of the IP core's (see col. 1, lines 42 et seq.). This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have been motivated to employ a method for testing embedded cores with the flexibility of reusing the IP cores.

Claim **11**:

De substantially teaches a system for testing an ASIC embedded core including proprietary and nonproprietary circuitry and customer supplied test patterns utilizing an automatic test pattern generation software generating scan vectors (see col. 1 line 12 seq.); the system comprising: scan flip-flops to create pseudo inputs to test a test shell

with unprotected data as well as a partial netlist wherein the partial netlist does not include the full circuitry and the partial netlist is based on gates that are isolated from the core (see col. 4, lines 54 et seq.). De also teaches testing the ASIC embedded core using a combination of the customer supplied test vectors and the partial netlist wherein patterns are generated by an automatic test generating software (see col. 8, lines 33 et seq).

De does not specifically teach adding customer supplied circuitry; however, Whetsel in an analogous art teaches an integrated circuit including an IP core and a user–added scan register connected via a test access port interface (see fig. 3, and col. 3, lines 20 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ASIC of De to include a user-added scan register as taught by Whetsel since, Whetsel teaches testing an IC with an embedded core and a user-added scan register provides greater flexibility in testing embedded cores. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have been motivated to employ a method wherein a customer has greater flexibility of testing an embedded core.

As per claim **12**, De teaches the using a scan chain to test the integrated circuit (see col. 5, lines 55 to 64).

As per claim **13**, De teaches an automatic test generating program generating test vectors to test the integrated circuit using the partial netlist (see col. 5, lines 20 to 35).

As per claim **14**, De teaches an integrated circuit including proprietary information; however, De fail to clearly tech the embedded core includes a JTAG interface. Whetsel teaches an embedded core including a test access port (TAP) (see fig. 3 and col. 3, lines 33 et seq.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the ASIC of De to include a test access port as taught by Whetsel since, Whetsel teaches testing an IC including an embedded core with a test access port is a known standard in the art as well as enables core reuse (see col. 1, lines 42 et seq.). This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have been motivated to employ a system for testing embedded cores that enables reuse as taught by Whetsel.

Allowable Subject Matter

7. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record teaches a method and an apparatus for testing embedded cores as detailed above; however, fails to specifically teach or fairly suggest or render obvious the step of stripping references to said at least one pseudo input form said total netlist as recited in dependent claim 9.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A. Chase whose telephone number is 571-272-3816. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).